AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1-32. (Cancelled)

33. (New) A circuit substrate comprising:

a substrate including a first surface and a second surface opposite to the first surface;

a first conductor pattern formed on the first surface; and

a second conductor pattern formed on the second surface,

wherein if the circuit substrate is mounted on a second substrate, the second surface is the surface mounted to the second substrate, and

the second surface has larger surface roughness than the first surface.

34. (New) A circuit substrate according to claim 33, further comprising an external terminal formed on the second conductor pattern.

35. (New) A circuit substrate according to claim 34, further comprising a device mounted on the first conductor pattern.

36. (New) A circuit substrate according to claim 34, wherein the external terminal is one of a ball-shaped solder, a pillar-shaped solder and a pin.

37. (New) A circuit substrate according to claim 33, further comprising a through hole in the substrate connecting the first and second surface.

38. (New) A circuit substrate according to claim 37, further comprising an electrode filled in the through hole.

39. (New) A circuit substrate according to claim 37, further comprising an electrode formed along the through hole.

40. (New) A circuit substrate according to claim 38, wherein the external terminal is connected directly underneath the electrode.

41. (New) A circuit substrate according to claim 39, further comprising a solder filled in the through hole.

42. (New) A circuit substrate according to claim 41, wherein the solder has a higher melting point than the external terminal.

43. (New) A circuit substrate according to claim 33, further comprising a dielectric layer formed on at least a portion of the first and/or second conductor patterns; and a third conductor pattern formed on the dielectric layer.

44. (New) A circuit substrate according to claim 33, further comprising a device mounted on the first conductor pattern.

45. (New) A circuit substrate according to claim 44 wherein the device is an LSI chip.

46. (New) A circuit substrate according to claim 33, wherein a portion of the first conductor pattern is thinner than the rest portion.

47. (New) A circuit substrate according to claim 46, further comprising a device mounted on the thinner portion of the first conductor pattern.

48. (New) A circuit substrate according to claim 33, wherein the substrate includes a conductor pattern therein.

49. (New) A circuit substrate according to claim 33, further comprising an insulator formed on the first and/or second conductor patterns.

50. (New) An apparatus including a circuit substrate comprising:

a circuit substrate comprising;

a first substrate including a first surface and a second surface opposite to the first surface,

a first conductor pattern formed on the first surface, and

a second conductor pattern formed on the second surface,

wherein the second surface has larger surface roughness than the first surface, and

a second substrate, wherein the circuit substrate is mounted on the second substrate via the second surface.

51. (New) An apparatus according to claim 50, further comprising an external terminal connecting the second conductor pattern and the second substrate.

52. (New) An apparatus according to claim 51, further comprising a device mounted on the first conductor pattern.